

CLAIMS

We claim:

1 1. A process for forming at least one interface region
2 between two regions of semiconductor material, the process
3 comprising:

4 forming at least one region of dielectric material
5 comprising nitrogen in the vicinity of at least a portion of
6 a boundary between the two regions of semiconductor
7 material, thereby controlling electrical resistance at the
8 interface.

1 2. The process according to claim 1, wherein the two
2 regions of semiconductor material each are selected from the
3 group consisting of monocrystalline silicon, polycrystalline
4 silicon, amorphous silicon, monocrystalline SiGe and
5 polycrystalline SiGe.

1 3. The process according to claim 1, wherein a first
2 of the two regions of semiconductor material is
3 monocrystalline silicon and a second of the regions of
4 semiconductor material is non-monocrystalline silicon.

1 4. The process according to claim 3, wherein the
2 second region of semiconductor material is amorphous
3 silicon.

1 5. The process according to claim 1, wherein the
2 dielectric material is N, Si_xN_y , or $\text{Si}_x\text{O}_y\text{N}_z$.

1 6. The process according to claim 1, wherein forming
2 the at least one region of dielectric material comprises:
3 implanting the dielectric material in the vicinity of
4 the surface of a first of the regions of semiconductor
5 material.

1 7. The process according to claim 6, wherein the
2 dielectric material is deposited at an energy sufficient to
3 create a discontinuous layer of dielectric material.

1 8. The process according to claim 6, wherein the
2 dielectric material is deposited at a thickness and covering
3 a portion of the boundary between the two regions of
4 semiconductor material sufficient to control base current
5 flowing between the two regions of semiconductor material.

1 9. The process according to claim 6, wherein the

2 dielectric material is implanted at the surface of the first
3 region of semiconductor material.

1 10. The process according to claim 6, wherein atoms or
2 molecules of the dielectric material are implanted at the
3 surface of one of the regions of semiconductor material.

1 11. The process according to claim 6, wherein atoms or
2 molecules of the dielectric material are implanted under the
3 surface of one of the regions of semiconductor material.

1 12. The process according to claim 6, wherein one of
2 the regions of semiconductor material is monocrystalline
3 silicon and the dielectric material includes nitrogen atoms
4 implanted in the monocrystalline silicon.

1 13. The process according to claim 12, wherein the
2 nitrogen atoms are implanted at an energy of about 0.1 KeV
3 to about 5 KeV.

1 14. The process according to claim 12, wherein the
2 nitrogen atoms are implanted at a dose of from about 1×10^{11}
3 to about 1×10^{14} and with an energy of about 0.1 KeV to
4 about 5 KeV.

1 15. The process according to claim 6, further
2 comprising:
3 subjecting the semiconductor material and the implanted
4 dielectric material to an annealing step.

1 16. The process according to claim 6, further
2 comprising:
3 utilizing a mask to selectively implant the dielectric
4 material in the semiconductor.

1 17. The process according to claim 6, further
2 comprising:
3 implanting a layer of the dielectric material; and
4 selectively removing portions of the dielectric
5 material.

1 18. The process according to claim 1, wherein forming
2 the at least one region of dielectric material comprises:
3 subjecting a first of the regions of semiconductor
4 material to a elevated temperatures and a nitrogen-
5 containing gaseous atmosphere.

1 19. The process according to claim 18, wherein the
2 gaseous atmosphere includes at least one gas selected from

3 the group consisting of N_2O , NO or NH_3 .

1 20. The process according to claim 18, wherein the
2 first region of semiconductor material is subjected to
3 temperatures of about $300^\circ C$ to about $1000^\circ C$.

1 21. The process according to claim 18, wherein the
2 first region of semiconductor material is subjected to the
3 elevated temperatures and gaseous atmosphere for a time of
4 about 1 second to about 60 seconds.

1 22. The process according to claim 18, wherein the at
2 least one region of dielectric material includes a
3 discontinuous film of Si_xN_y , or $Si_xO_yN_z$.

1 23. The process according to claim 18, wherein the
2 first region of semiconductor material is monocrystalline
3 silicon.

1 24. The process according to claim 18, wherein
2 exposing the first region of semiconductor material to the
3 elevated temperatures includes ramping the temperature up a
4 process temperature.

1 25. The process according to claim 24, wherein the
2 temperature is ramped up at a rate of about 5° C per second
3 to about 100° C per second to a temperature of about 400° C
4 to about 800° C.

1 26. The process according to claim 24, wherein
2 subjecting the first semiconductor material to a gaseous
3 atmosphere includes subjecting the first semiconductor
4 material to a NH₃ gas flowing at a rate of about 5 SLPM for
5 about 5 to about 15 seconds.

1 27. The process according to claim 18, further
2 comprising:
3 ramping down the temperature to ambient temperature
4 after subjecting the first semiconductor material to
5 elevated temperature.

1 28. The process according to claim 27, wherein the
2 temperature is ramped down at a rate of about 15° C to about
3 30° C.

1 29. The process according to claim 24, further
2 comprising:
3 ramping down the temperature to ambient temperature

4 after subjecting the first semiconductor material to
5 elevated temperature.

1 30. The process according to claim 18, wherein the
2 process creates a discontinuous layer of dielectric material
3 having a thickness of about 1 Å to about 10 Å on the first
4 region of semiconductor material.

1 31. The process according to claim 18, further
2 comprising:
3 depositing a second region of semiconductor material on
4 the first region of semiconductor material.

1 32. The process according to claim 30, further
2 comprising:
3 removing portions of the dielectric material at least
4 one of during and after deposition of the second region of
5 semiconductor material.

1 33. The process according to claim 18, wherein the
2 first region of semiconductor is exposed to elevated
3 temperatures and nitrogen-containing gaseous atmosphere by a
4 rapid thermal process or a conventional furnace process.

1 34. The process according to claim 1, wherein forming
2 the at least one region of dielectric material comprises:
3 depositing a discontinuous film of the dielectric
4 material by a chemical vapor deposition process.

1 35. The process according to claim 33, wherein the
2 chemical vapor deposition process is a low pressure chemical
3 vapor deposition process or a plasma enhanced chemical vapor
4 deposition process.

1 36. The process according to claim 33, wherein the
2 chemical vapor deposition process is carried out using
3 silane or dichlorosilane with NH_3 or N_2O .

1 37. The process according to claim 33, wherein the
2 film has a thickness of about 1 Å to about 10 Å.

1 38. The process according to claim 33, wherein the
2 film has a thickness of less than one monolayer.

1 39. The process according to claim 33, wherein the
2 chemical vapor deposition is carried out at a temperature of
3 about 600° C to about 800° C.

1 40. The process according to claim 33, wherein
2 deposition gases flow for less than about 5 seconds.

1 41. The process according to claim 33, wherein the
2 chemical vapor deposition process utilizes at least one
3 silicon source gas and at least one nitrogen/oxygen source
4 gas and a ratio of silicon source gas to nitrogen/oxygen
5 source gas is controlled to produce a desired silicon-
6 nitrogen/oxygen stoichiometry.

1 42. The process according to claim 1, wherein the at
2 least one region of dielectric material is deposited on a
3 sidewall of a trench.

1 43. The process according to claim 1, wherein the
2 dielectric material further comprises at least one oxide.

1 44. A semiconductor device prepared by a process
2 comprising:
3 forming at least one region of dielectric material in
4 the vicinity of at least a portion of a boundary between the
5 two regions of semiconductor material, thereby controlling
6 electrical resistance at the interface, the dielectric
7 material including nitrogen.

1 45. A semiconductor device, comprising:
2 a region of a first semiconductor material;
3 a region of a second semiconductor material; and
4 an interface region including at least one region of
5 dielectric material comprising nitrogen in the vicinity of
6 at least a portion of a boundary between the first region of
7 semiconductor material and the second region of
8 semiconductor material, thereby controlling electrical
9 resistance at the interface.

1 46. The semiconductor device according to claim 45,
2 wherein the first region of semiconductor material and the
3 second region of semiconductor material are selected from
4 the group consisting of monocrystalline silicon,
5 polycrystalline silicon, amorphous silicon, polycrystalline
6 SiGe and monocrystalline SiGe.

1 47. The semiconductor device according to claim 45,
2 wherein a first of the two regions of semiconductor material
3 is monocrystalline silicon and a second of the regions of
4 semiconductor material is non-monocrystalline silicon.

1 48. The semiconductor device according to claim 47,
2 wherein the second region of semiconductor material is

3 amorphous silicon.

1 49. The semiconductor device according to claim 45,
2 wherein the dielectric material is N, Si_xN_y , or $\text{Si}_x\text{O}_y\text{N}_z$.

1 50. The semiconductor device according to claim 45,
2 wherein the dielectric material is implanted at the surface
3 of the first region of semiconductor material.

1 51. The semiconductor device according to claim 45,
2 wherein atoms of the dielectric material are implanted at
3 the surface of one of the regions of semiconductor material.

1 52. The semiconductor device according to claim 45,
2 wherein atoms of the dielectric material are implanted under
3 the surface of one of the regions of semiconductor material.

1 53. The semiconductor device according to claim 45,
2 wherein one of the regions of semiconductor material is
3 monocrystalline silicon and the dielectric material includes
4 nitrogen atoms implanted in the monocrystalline silicon.

1 54. The semiconductor device according to claim 45,
2 wherein the at least one region of dielectric material is a

3 discontinuous film.

1 55. The semiconductor device according to claim 54,
2 wherein the film is silicon nitride or silicon oxynitride.

1 56. The semiconductor device according to claim 54,
2 wherein the film of dielectric material has a thickness of
3 about 1 Å to about 10 Å.

1 57. The semiconductor device according to claim 54,
2 wherein the film of dielectric material has a thickness of
3 less than one monolayer.

1 58. The semiconductor device according to claim 45,
2 wherein the at least one region of dielectric material is
3 arranged on a sidewall of a trench in monocrystalline
4 silicon, the trench being filled with non-monocrystalline
5 silicon.

1 59. The semiconductor device according to claim 45,
2 wherein the dielectric further comprises at least one oxide.